REMARKS

Claims 1-5, 10 and 16-18 have been amended to improve form, claim 6 has been canceled without prejudice or disclaimer and new claims 21-23 have been added. Claims 1-5, 7, 9-13, 15-19 and 21-23 are now pending in this application.

Initially, the applicants wish to thank Examiner Bates and Supervisory Examiner Najjar for the courtesy extended in the personal interview on August 9, 2005. To briefly summarize the interview, features of claims 1 and 10 were discussed with respect to the applied references. The applicants' attorney indicated that none of the applied references disclosed the features recited in, for example, claim 10. The applicants' attorney also indicated that an amendment clarifying the language of claim 10 may be made in a subsequent response and that similar clarifying amendments may be made in other claims, such as claim 1. The Examiners indicated that the rejections based on the applied references would be reconsidered in light of any such clarifying amendments.

Claims 10-13 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Bass et al. (U.S. Patent No. 6,460,120; hereinafter Bass) in view of Humphrey et al. (U.S. Patent No. 4,933,846; hereinafter Humphrey). The rejection is respectfully traversed.

Initially, based on the actual rejection at pages 3-4 of the Office Action, it is believed that the Examiner intended to reject claims 10, 11, 13 and 15 based on the combination of Bass and Humphrey and inadvertently listed claim 12 in the grounds of rejection at page 2 of the Office Action (as opposed to claim 15). If this is not the case, the applicants respectfully request clarification as to the grounds of rejection in any subsequent Office Action.

In any event, claim 10, as amended, recite that the simultaneously transferring includes alternating the transferring of data frame information from a first group of the receive devices to the first and second memories, and alternating the transferring of data frame information from a second group of the receive devices to the first and second memories. Claim 10, as amended, further recites that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories. The cited references, taken singly or in combination, do not disclose or suggest these features.

For example, the Office Action admits that Bass does not disclose alternately transferring data frame information from a first group of receive devices to first and second memories or alternately transferring data frame information from a second group of receive devices to first and second memories (Office Action – page 3). The Office Action, however, states that Humphrey discloses alternately transferring data frame information from a first group of receive devices to first and second memories and alternately transferring data frame information from a second group of receive devices to first and second memories and points to col. 5, lines 44-63 of Humphrey for support (Office Action – page 3). The applicants respectfully disagree.

Initially, the applicants note that claim 10, as amended, recites "alternating the transfer of data frame information", as opposed to "alternately transferring data frame information". As discussed in the personal interview, this clarification is made to more clearly represent the claimed transferring.

In any event, Humphrey at col. 5, lines 44-63 discloses that each memory cycle has two phases. During the first phase, the enabled processor puts identical addresses on both the A and B common buses 102 and 104 while 16-bit processors access only their dedicated common bus. During the second phase, data from the addressed memory cell is read on either the A read bus, B read bus or concurrently on both the A and B buses. In the event of a write cycle, the write data is placed on the respective common bus (Humphrey – col. 4, lines 44-54 and Fig. 1). This portion of Humphrey further discloses that both processors 114 and 116, or processors 116 and 118, might operate concurrently during a given memory cycle over their respective A and B buses. To accomplish this, node control 130 places the processor slot ID code associated with processor 114 on the A section of the slot processor ID bus and places the processor ID code associated with processor 116 on the B portion of the slot processor bus (Humphrey – col. 5, lines 55-63).

These portions of Humphrey do not disclose or suggest alternating the transferring of data frame information from a first group of the receive devices to the first and second memories, and alternating the transferring of data frame information from a second group of the receive devices to the first and second memories, much less that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories, as recited in amended claim 10. In contrast, these portions of Humphrey merely disclose a method in which one of processors 110-118 accesses one of buses 102-108 during a read or write cycle. Humphrey clearly does not disclose alternating the transferring of data frame information from a first group of receive devices to first and second memories or alternating the transferring of data

frame information from a second group of receive devices to the first and second group of memories, as recited in amended claim 10.

The applicants further note that Humphrey at col. 8, lines 25-62 (discussed during the personal interview) discloses a channel bandwidth allocation scheme. In particular, this portion of Humphrey discloses:

> Each time-slot corresponds to one central memory cycle time, which is nominally 80 nanoseconds. Thus, the total time for the entire 16 time slots is 1.28 microseconds. This means that each time a processor gains access to one of the 16-bit buses A or B in a given time slot, it provides a channel data rate of 25 megabits per second. The aggregate data rate for all 16 time slots and both A and B buses is 400 megabits per second. In this hypothetical example, processor 1, a 32-bit processor, is shown as connected to both bus A and bus B and is granted access in time slots 1 and 5, thus providing a total channel bandwidth of 100 megabits per second. It should be noted that for 32-bit processors, the lower 16 bits of data are always connected to Memory Bank 0 and the upper 16 bits of data are always connected to Bank 1. Processor 2 is assumed to be a 16-bit processor and is connected only to bus A and is granted time slots 3 and 7, providing a 50 megabit data rate. Processor 3 is illustrated as a 16-bit processor and is connected only to bus B. It is allocated time slots 3 to communicate with Bank 0 and time slot 7 to communicate with Bank 1. Memory Banks 0 and 1 are switched between buses A and B by the aforementioned Bus/Bank select switch 138. Processor 4 is shown as a 16-bit processor arbitrarily connected only to bus A. It, along with processor 3, is allocated time slots 2, 4, 6 and 8, each processor accessing a different bank, i.e., processor 4 to Bank 0 during slot 2 and 6 and to Bank 1 during slots 4 and 8. In this way, memory exchanges between the Central Memory 100 and processors 4 and 5 can be interleaved, with each processor granted a 100 megabit per second bandwidth. One restriction which must be observed is that each 16-bit processor must be given at least two time slots, one in which to access Bank 0 and one in which to access Bank 1. A 32-bit processor, since it simultaneously accesses both banks, may be allocated as little as one time slot.

This portion of Humphrey has nothing to do with alternating the transferring of data frame information <u>from a first group of receive devices to first and second memories</u> or alternating the transferring data frame information <u>from a second group of receive devices to the first and second memories</u>, much less that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data

frame information from the first group of receive devices is being transferred to the other of the first and second memories, as recited in amended claim 10. In contrast, this portion of Humphrey merely discloses that a number of processors may be assigned slots in an arbitration cycle, but does not disclose or suggest that any of the processors access the same first and second memories in an alternating manner as recited in claim 10.

In particular, Humphrey at col. 8, lines 49-55 (pointed to in the personal interview by the Examiners) discloses that "Processor 4 is shown as a 16-bit processor arbitrarily connected only to bus A. It, along with processor 3, is allocated time slots 2, 4, 6 and 8, each processor accessing a different bank, i.e., processor 4 to Bank 0 during slot 2 and 6 and to Bank 1 during slots 4 and 8. In this way, memory exchanges between the Central Memory 100 and processors 4 and 5 can be interleaved." As best understood by the applicants, this portion of Humphrey in conjunction with Table II at col. 8, lines 15-25 of Humphrey discloses that accesses to memory 100 may be interleaved during a channel bandwidth allocation cycle. This portion of Humphrey, however, does not disclose or suggest that any of the processors in Humphrey receive data frame information and alternate the transfer of data frame information from a first group of receive devices to first and second memories or alternate the transfer of data frame information from a second group of receive devices to the first and second memories, much less that when data frame information from the second group of receive devices is being transferred to one of the first and second memories, data frame information from the first group of receive devices is being transferred to the other of the first and second memories, as required by amended claim 10. In contrast, this portion of Humphrey merely discloses that particular processors may receive access to memory 100 during particular slots. Nowhere in this portion of Humphrey, or elsewhere, does Humphrey

disclose or suggest transferring data from a first group of receive devices and from a second group of receive devices to first and second memories in an alternating manner, as recited in amended claim 10.

For at least the reasons discussed above, the combination of Bass and Humphrey does not disclose or suggest each of the features of claim 10. Accordingly, withdrawal of the rejection and allowance of claim 10 are respectfully requested.

Claims 11, 13 and 15 are dependent on claim 10 and are believed to be allowable for at least the reasons claim 10 is allowable. Accordingly, withdrawal of the rejection and allowance of claims 11, 13 and 15 are respectively requested.

Claims 1-6, 9, 12 and 16-19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Bass in view of Humphrey and further in view of Mann (U.S. Patent No. 6,021,477). The rejection is respectfully traversed.

Claim 1, as amended, recites features similar to claim 10. For reasons similar to those discussed above with respect to claim 10, the combination of Bass and Humphrey does not disclose or suggest each of the features of amended claim 1. Mann has been used in the rejection to allegedly disclose generating odd and even address information when transferring data to first and second memories. Mann, however, does not remedy the deficiencies in the combination of Bass and Humphrey with respect to amended claim 1.

For at least these reasons, the combination of Bass, Humphrey and Mann does not disclose or suggest each of the features of amended claim 1.

In addition, even if, for the sake of argument, the combination of the three references could be fairly construed to disclose or suggest each of the features of claim 1, the

applicants assert that the motivation to combine these three references does not satisfy the requirements of 35 U.S.C. § 103.

For example, the Office Action states that it would have been obvious to combine Humphrey with Bass "in order to allow multiple devices and ports to communicate in the same device at a higher throughput" (Office Action – page 5). The Office Action further states that it would have been obvious to combine Mann with Bass "in order to allow fixed bus length systems work store information double that fixed bus length using dual memories" (Office Action – page 6). These alleged motivations are merely conclusory statements providing alleged benefits of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103. The applicants further assert that the only motivation for combining these disparate references is based on impermissible hindsight.

Claims 2-5 and 9 are dependent on claim 1 and are believed to be allowable for at least the reasons claim 1 is allowable. Accordingly, withdrawal of the rejection and allowance of claim 2-5 and 9 are respectfully requested.

Claim 16, as amended, recites features similar to claim 1. For reasons similar to those discussed above with respect to claim 1, the combination of Bass, Humphrey and Mann does not disclose or suggest each of the features of claim 16. In addition, the applicants assert that the motivation for combining these three references does not satisfy the requirements of 35 U.S.C. § 103.

For at least these reasons, withdrawal of the rejection and allowance of claim 16 are respectfully requested.

Claims 17-19 are dependent on claim 16 and are believed to be allowable for at least the reasons claim 16 is allowable. Accordingly, withdrawal of the rejection and allowance of claims 17-19 are respectfully requested.

Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell et al. (U.S. Patent No. 6,208,650; hereinafter Hassell) in view of Springer et al. (U.S. Patent No. 4,247,920; hereinafter Springer) in further view of Gayton et al. (U.S. Patent No. 5,680,401; hereinafter Gayton) and further in view of Runaldue et al. (U.S. Patent No. 6,052,751; hereinafter Runaldue). The rejection is respectfully traversed.

Initially, based on the actual rejection at page 10 of the Office Action, it is believed that the Examiner intended to reject claim 7 based on the combination of Bass, Humphrey, Mann and Runaldue since Hassell, Springer and Gayton (used in the previous rejection) were not referenced in the actual rejection in this Office Action. If this is not the case, the applicants respectfully request clarification as to the grounds of rejection in any subsequent Office Action.

In any event, claim 7 is dependent on claim 1 and is believed to be allowable for at least the reasons claim 1 is allowable. Runaldue does not make up for the deficiencies in the combination of Bass, Humphrey and Mann discussed above with respect to claim 1. Accordingly, withdrawal of the rejection and allowance of claim 7 are respectfully requested.

NEW CLAIMS

New claims 21-23 have been added. These claims are dependent on claims 1, 10 and 16, respectively and are believed to be allowable for at least the reasons their respective

independent claims are allowable. In addition, these claims recite additional features not disclosed or suggested by the cited art.

For example, claim 21 recites that the external memory interface is further configured to transfer data from one of the first group of receive devices to the first memory during a first clock cycle, transfer data from one of the second group of receive devices to the second memory during the first clock, transfer data from one of the first group of receive devices to the second memory during a second clock cycle, the second clock cycle immediately succeeding the first clock cycle and transfer data from one of the second group of receive devices to the first memory during the second clock cycle. The cited art does not disclose or suggest these features.

Claim 22 recite that the alternating of the transferring of data frame information from the first group of receive devices to the first and second memories is performed each clock cycle. The cited art does not disclose or suggest this feature.

Claim 23 recites that the switching device is further configured to alternate the transfer of data frame information from the first group of receive devices to the first and second external memory buses each clock cycle and alternate the transfer of data frame information from the second group of receive devices to the first and second external memory buses each clock cycle. The cited art does not disclose or suggest these features.

CONCLUSION

In view of the foregoing amendments and remarks, the applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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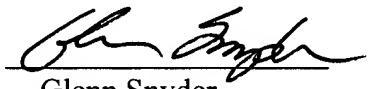
By: 
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